PCIe DMA mechanism

ISA - PCI - PCIe development history

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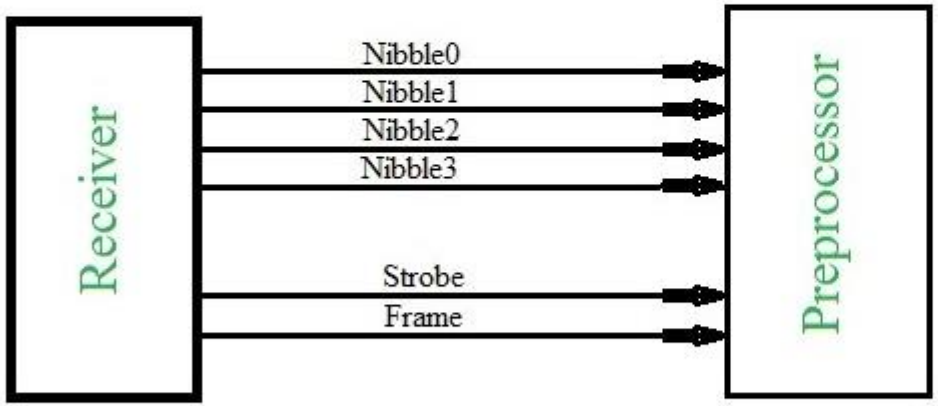
Receiver data bus

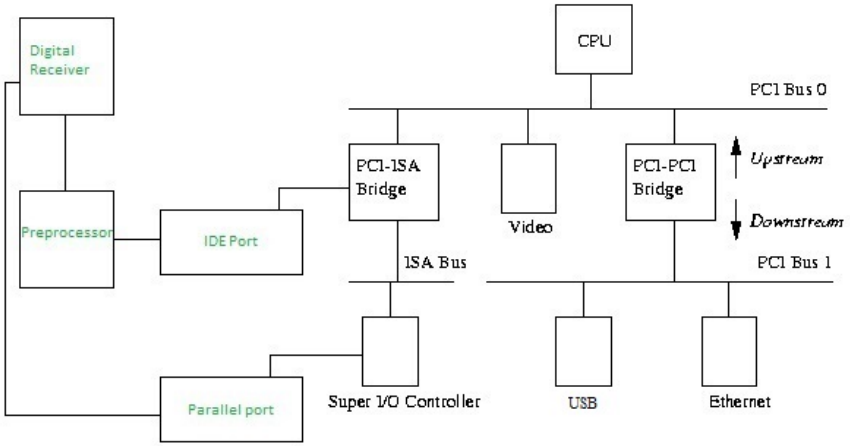
4 x 4 = 16 bits



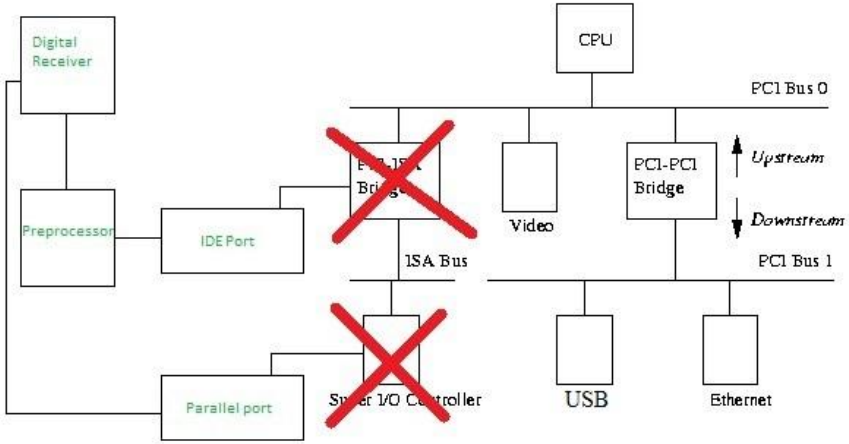
44 to 96 pins

Bandwith - 30 kHz
Digital form - 60 kHz
I & Q - 120 kHz
Nibbles - 480 kHz
4 channels - 1920 kHz

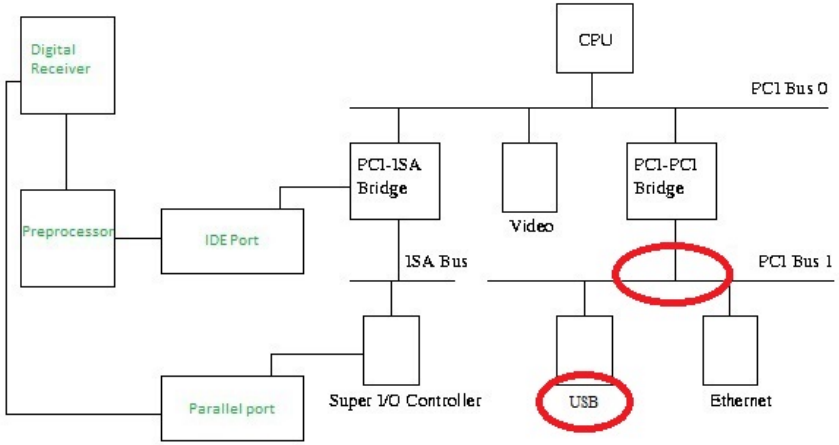
Current system



Obsolete system components

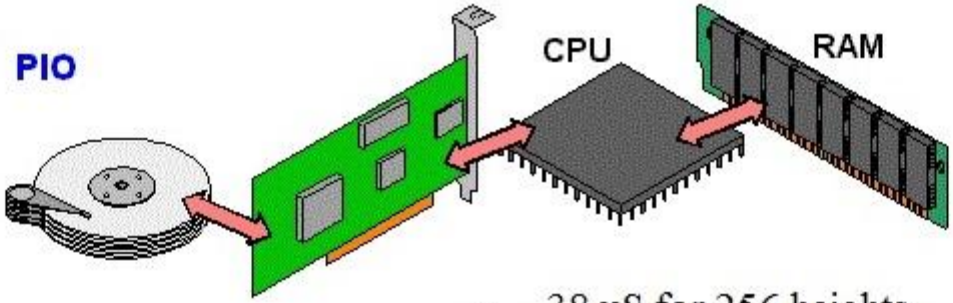


Why PCI?

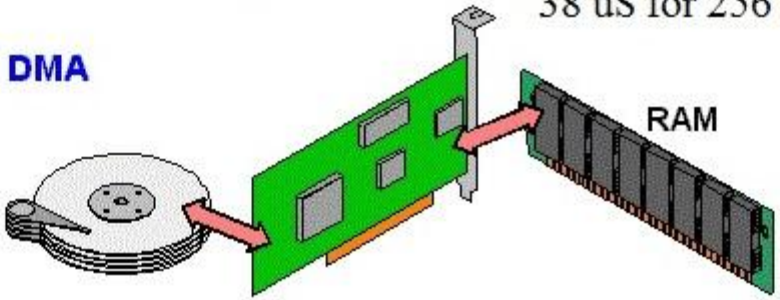


PCI DMA

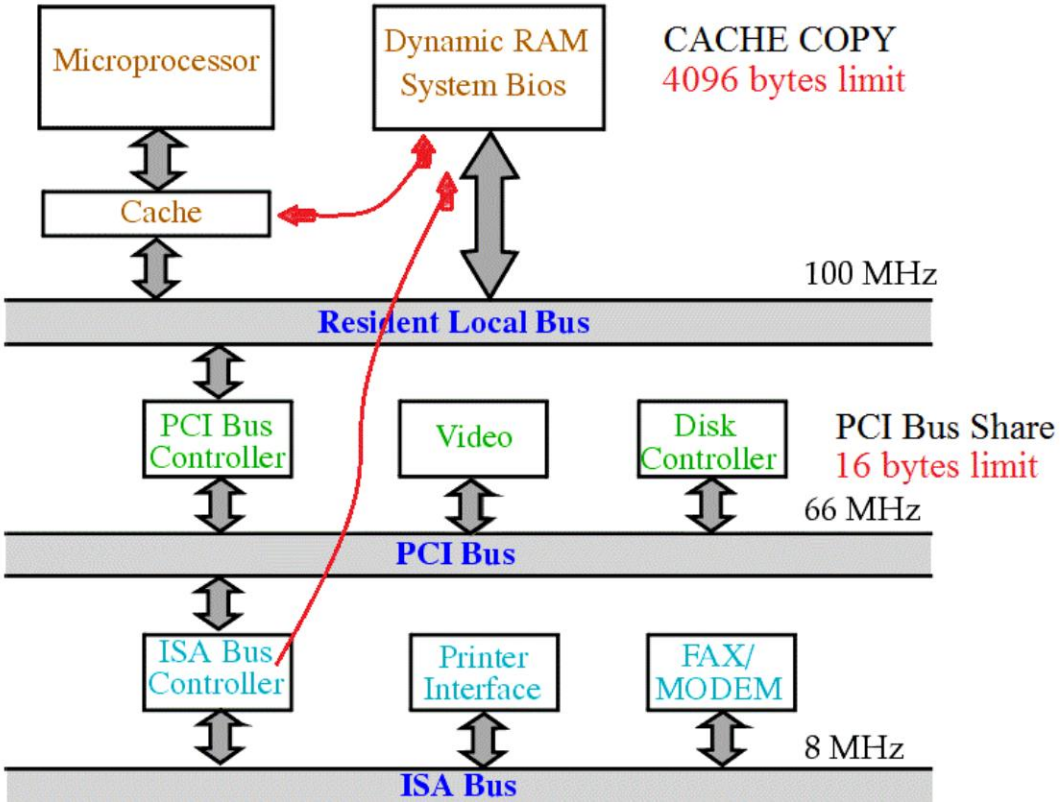
2.2 mS for 256 heights



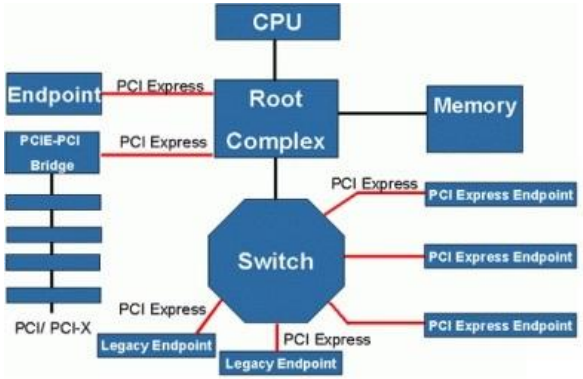
38 uS for 256 heights

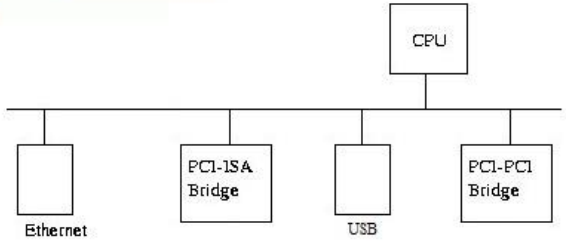


PC Memory Specific

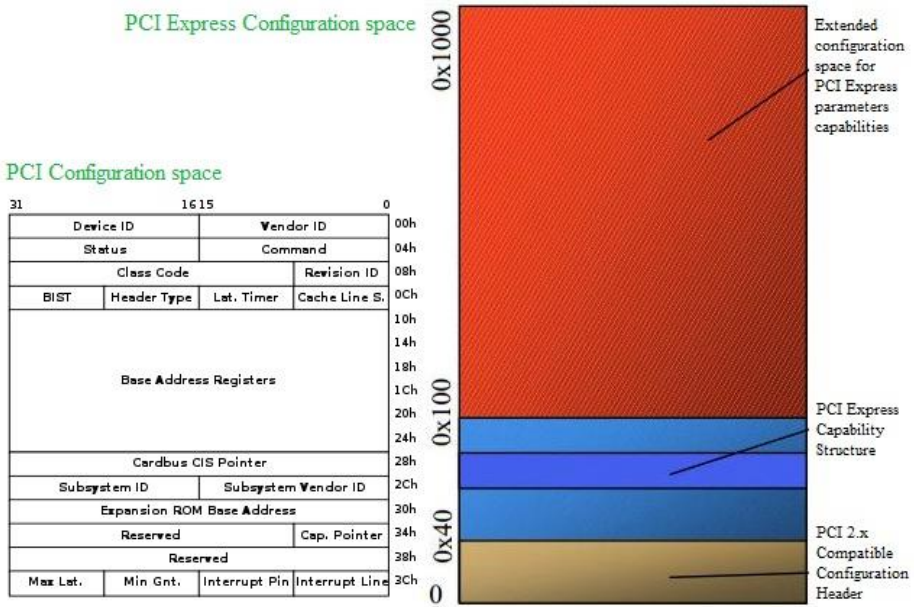


PCI vs PCI Express

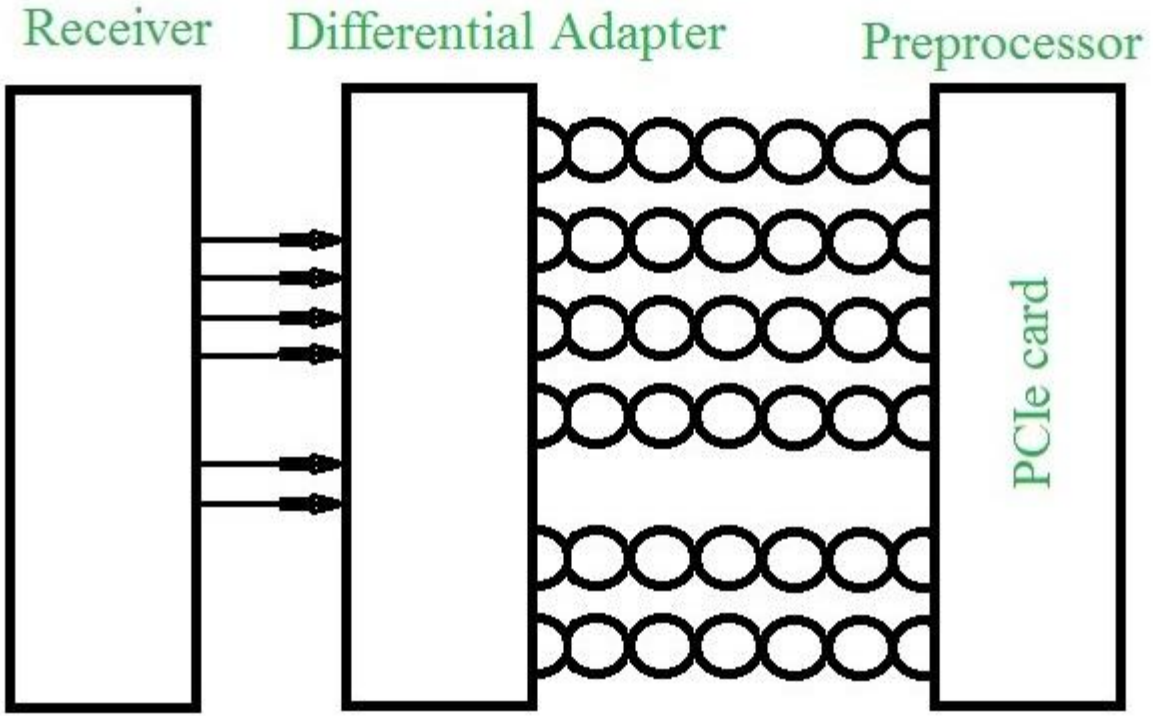




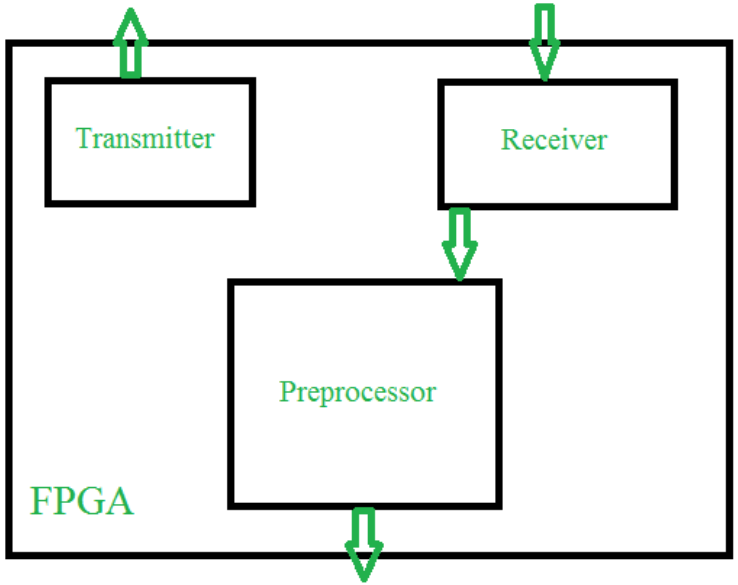
PCI vs PCIe


PCI Express Configuration space
PCI Configuration space
31
16 15
0
Device ID
Vendor ID
Status
Command
Class Code
Revision ID
BIST
Header Type
Lat. Timer
Cache Line S.
Base Address Registers
Cardbus CIS Pointer
Subsystem ID
Subsystem Vendor ID
Expansion ROM Base Address
Reserved
Cap. Pointer
Reserved
Max Lat.
Min Gnt.
Interrupt Pin
Interrupt Line
00h
04h
08h
0Ch
10h
14h
18h
1Ch
20h
24h
28h
2Ch
30h
34h
38h
3Ch
0x1000
0x100
0x40
0
Extended configuration space for PCI Express parameters capabilities
PCI Express Capability Structure
PCI 2.x Compatible Configuration Header

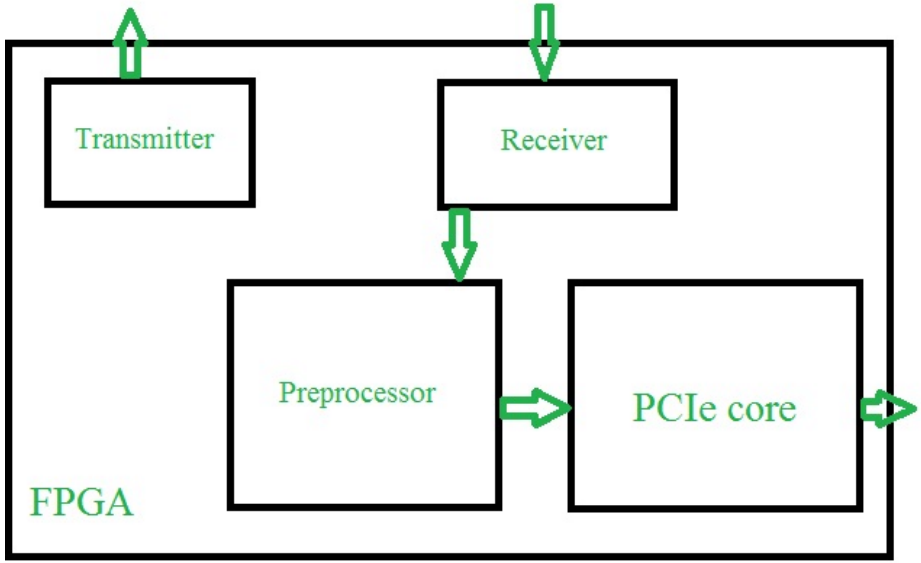
DPS-4D Upgrade



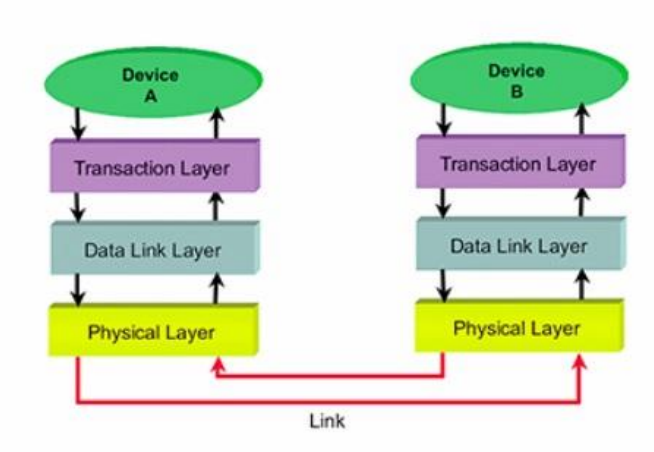
FPGA solution



Xilinx solution



PCIe (serial)



Serial interface

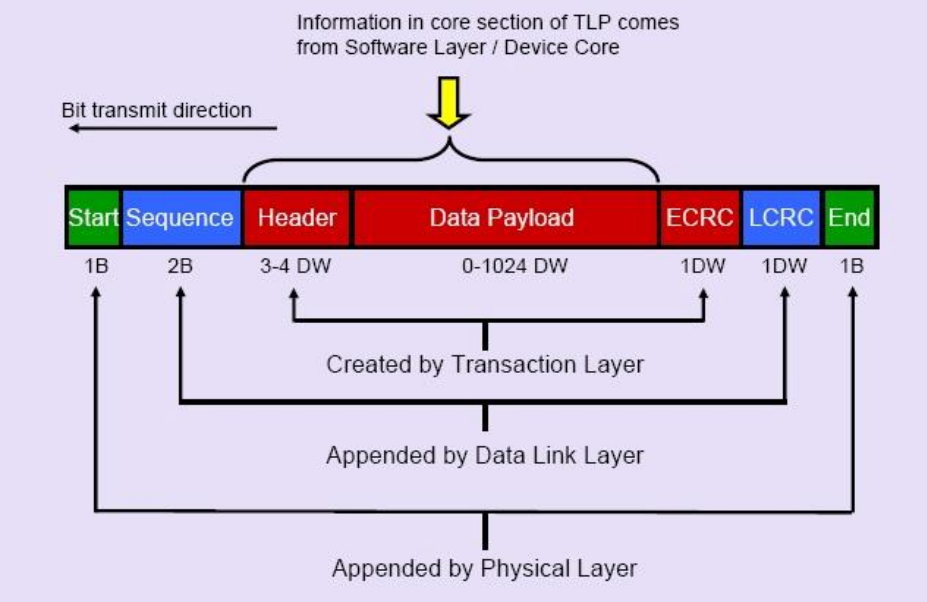
1. TLP (header-data-CRC(optionally))

2. Link management (CRC,errors)

(re-send, TLP number)

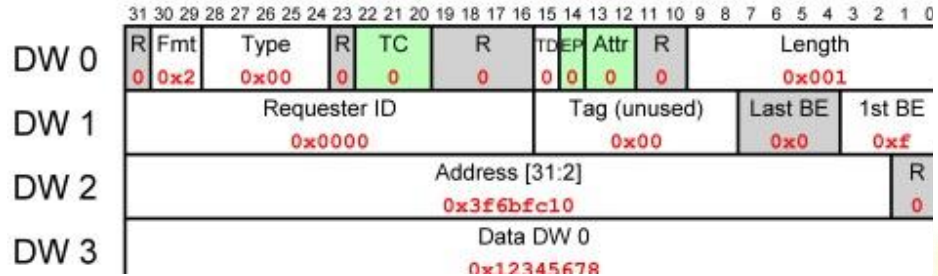
3. Start-stop (1B_____1B)

PCIe packet



Transactions:

1. Memory
2. I/O
3. Configuration
4. Message (NEW!)



PCIe DMA

Step	Operation	Register Operation	Value
1	Assert Initiator Reset	PIO Write DCR1	0x00000001
2	De-assert Initiator Reset	PIO Write DCR1	0x00000000
3	Write DMA H/W Address	PIO Write WDMATLPA	H/W Address
4	Write DMA TLP Size	PIO Write WDMATLPS	Write TLP Size
5	Write DMA TLP Count	PIO Write WDMATLPC	Write TLP Count
6	TLP Payload Pattern	PIO Write WDMATLPP	Data Pattern
7	Write DMA Start	PIO Write DCR2	0x00000001
8	Wait for Interrupt TLP		
9	Write DMA Performance	PIO Read WDMAPERF	

Write DMA Sequence of Events